|  |  |  |  |
| --- | --- | --- | --- |
| Cases | A | B | C\_IN |
| A | 10011111111111111111111111111101  (-1610612739) | 11011111111111111111111111111110  (-536870914) | 0 |
| B | 11011111111111111111111111111101  (-536870915) | 11011111111111111111111111111110  (-536870914) | 0 |
| C | 01000000000000000000000000000010  (1073741826) | 01000000000000000000000000000000  (1073741824) | 0 |
| D | 00000000010000000000000000100000  (4194336) | 00000000000000000000000100000011  (259) | 0 |
| E | 01000000000000000000000000000010  (1073741826) | 11001011100010101100100111111010  (-880096774) | 0 |
| F | 11001011100010101100100111111011  (-880096773) | 01000000000000000000000000000010  (1073741826) | 1 |
| G | 11111111111111111111111111111110  (-2) | 00000000000000000000000000000001  (1) | 1 |
| H | 00000001010101001101000101010000  (22335824) | 11111111000000000000000000000000  (-16777216) | 0 |
| I | 00000001010101001101000101010000  (22335824) | 01111111000000000000000000000000  (2130706432) | 0 |
| Cases | SUM | C\_OUT | V |
| A | 01111111111111111111111111111011  (2147483643) | 1 | 1 |
| B | 10111111111111111111111111111011  (-1073741829) | 1 | 0 |
| C | 10000000000000000000000000000010  (-2147483646) | 0 | 1 |
| D | 00000000010000000000000100100011  (4194595) | 0 | 0 |
| E | 00001011100010101100100111111100  (193645052) | 1 | 0 |
| F | 00001011100010101100100111111110  (193645054) | 1 | 0 |
| G | 00000000000000000000000000000000  (0) (Worst case delay = 452ns) | 1 | 0 |
| H | 00000000010101001101000101010000  (5558608) | 1 | 0 |
| I | 10000000010101001101000101010000  (-2141925040) | 0 | 1 |

The test procedure for the 32-Bit Ripple Carry Adder was adapted from the provided 3 bit ripple carry adder, and thus showed cases of negative + negative that set and don’t set the overflow flag, positive + positive that set and don’t set the overflow flag, positive + negative and negative + positive.

I also found the worst-case propagation delay for the adder, which is when every bit addition results in a carry into the next bit. Bit 0 is 1 + 1, which results in a delay of 18ns, as the signal must go through an XOR gate (4ns), AND gate (5ns) and OR gate (9ns), which has a carry into the next bit. The same happens for the next 31 bits, but the first XOR gate of every bit happen simultaneously, so bits 1 – 31 have a delay of 14ns. Therefore, the worst-case propagation delay is 18 + (14\*31) = 452ns.

I also found two numbers that, when added to the binary representation of my student number, would set the C flag and the V flag, as seen in cases H and I.